Tuesday, December 12, 2023

Session T-I

8:20 - 8:30

Opening Remarks

Room: Conference Hall

Session T-II

8:30 - 9:00

Keynote-1: Artificial Intelligence as an Enabler for 5G and Beyond 5G Communication Systems

Room: Conference Hall

Speaker: Pawan Fowdur

Session T-III

9:00 - 10:20

Electrical and Renewable Energy Systems

Room: Conference Hall

- T-III.1. **Adaptation of Interconnection Policy for DGs to Increase Renewable Energy Integration in Mauritius**

  Noormahmad Goolam Hossen, Robert T. F. Ah King   University of Mauritius

- T-III.2. **Modeling and Analysis of Load Balancing and Demand Response in Renewable Energy Infrastructures**

  Anshu Murdan   University of Mauritius

- T-III.3. **Evaluation of efficiency and power quality for a two-phase asymmetrical induction motor drive**

  Iqbal Jahmeerbacus, Anshu Murdan   University of Mauritius

- T-III.4. **Effects of Generator Order and Excitation Systems on Voltage Control**

  Naadia Hanaan Fokeerbux, Rajeshree Ramjug-Ballgobin   University of Mauritius

10:20 - 10:40   T-IV: Coffee Break

Session T-V

> **Advanced Packaging**

10:40 - 12:00
> Room: Conference Hall

- T-V.1. **Signal & Power Integrity Analysis and Solutions for HBM Gen3**

  Mukesh Moorthy, Hisham Abed   Synopsys Inc

- T-V.2. **The Significance of Thermal-Aware Universal Chiplet Interconnect Express (UCIe) Interface Design in 2.5D/3D ICs**

  Keeyoung Son, Keunwoo Kim, Jiwon Yoon,
  Seonguk Choi, Jihun Kim, Jonghyun Hong,   KAIST
  Junghyun Lee, Joungho Kim, Hyunwoo Kim

- T-V.3. **Thermal Analysis of High Bandwidth Memory (HBM)-GPU Module considering Power Consumption**

  Son Keeyoung[*], Park Joonsang[*], Kim Seongguk[*],
  Sim Boogyo[*], Kim Keunwoo[*], Choi Seonguk[*],   [*]KAIST, [+]SK hynix Inc.
  Kim Hyunsik[+], Kim Joungho[*]

- T-V.4. **Signal Integrity Design and Analysis of Universal Chiplet Interconnect Express (UCIe) Channel in Silicon Interposer for Advanced Package**

  Hyunwook Park[*], Boogyo Sim[+], Seongguk Kim[+],   [*]Missouri University of Science and
  Jihun Kim[+], Seongguk Choi[+], Joonsang Park[+],   Technology (MST), [+]Korea
  Jaehyup Kim[**], Joung Won Park[**], Daehyun   Advanced Institute of Science and
  Kang[**], Jinwook Song[++], Joungho Kim[+], Taein   Technology (KAIST), [**]Samsung
  Shin[+], Keunwoo Kim[+]   Semiconductor Inc., [++]Samsung
                                                                              Electronics

Session T-VI

> **EDA-1: MZ Technologies**

12:00 - 12:30
> Room: Conference Hall

An Innovative Advanced Packaging Approach That Boosts Device Miniaturization - Anna Fontanelli

12:30 - 1:15   T-VII: Lunch

Session T-VIII

              EDA-2: Cadence

1:15 - 1:30

              Room: Conference Hall

Challenges and Opportunities as Chips Transform into Systems - John Park

Session T-IX

              Keynote-2: Engineering AI-based intelligent mitigation and adaptation climate solutions for promoting sustainability in the built environment

1:30 - 2:00

              Room: Conference Hall

Speaker: Kishan Gooroochurn

Session T-X

              Poster Session

2:00 - 3:00

              Room: Conference Hall

Session T-XI

              AI/ML for Packaging

3:00 - 4:20

              Room: Conference Hall

- T-X.1. **Optimization of Eye Diagram Characteristics of MLGNR Interconnect Networks Using Fast ML Assisted Evolutionary Algorithm**

  Km Dimple, M. Ehteshamuddin, Surila Guglani, Avirup Dasgupta, Sourajeet Roy   IIT Roorkee

- T-X.2. **Noise-Aware Uncertainty Quantification of MLGNR Interconnects using Fast Trained Artifical Neural Networks**

  Asha Kumari Jakhar, Surila Guglani, Avirup Dasgupta, Sourajeet Roy   IIT Roorkee

- T-X.3. **Imitation Learning-based Equalizer Design Optimization Method on PCIe 6.0**

Jihun Kim, Seonguk Choi, Taein Shin, Keeyoung Son, Boogyo Sim, Seoungguk Kim, Haeyeon Kim, Joonsang Park, Jinwook Song, Kyungsuk Kim, Jonggyu Park, Joungho Kim	Korea Advanced Institute of Science and Technology (KAIST)

- T-X.4. **A Stochastic Active Learning Strategy for Gaussian Process Models with Application to the Uncertainty Quantification of Signal Integrity**

Paolo Manfredi	Politecnico di Torino

4:20 - 4:30   T-XI: Coffee Break

Session T-XIII

System-level EMI/EMC

4:30 - 5:50

Room: Conference Hall

- T-XII.1. **Multi-Objective EMI Optimisation using a Metamodel-based SiC/GaN Converter and NSGA II**

Jason Gomez[*], Suguna Sree Nukala[+], Akash [+], Dipanjan Gope[+], Jan Hansen[**]	[*]Indian Institute of Technology, Mumbai, India, [+]Indian Institute of Science, Bengaluru, India, [**]Institute of Electronics, Inffeldgasse 12/I, A-8010 Graz, Austria

- T-XII.2. **Comparison of Surrogate Modeling Approaches for Estimation of EMI Filter Insertion Loss**

Ayush Shukla[*], Suguna Sree Nukala[+], Akash [+], Dhiraj Kumar Singh[**], Dipanjan Gope[+], Jan Hansen[++]	[*]Manipal Institute of Technology, India, [+]Indian Institute of Science, India, [**]LRDE,DRDO, [++]Institute of Electronics, Austria

- T-XII.3. **EMI Performance of Multilayered Al-CoTaZr Films in Shielded Power Inductors**

Ghaleb Saleh Ghaleb Al-Duhni[*], Mudit Khasgiwala[+], Pulugurtha Markondeya Raj[*]	[*]Florida International University, [+]Applied materials

- T-XII.4. **Bulk Current Injection (BCI) Simulation and Measurement Correlation of an Automotive Battery Cell Voltages and Temperature Monitor IC**

Jie Chen[*], Rajen Murugan[*], Vishnu Ravinuthula[*], Willy Bristiel[*], Taylor Vogt[*], Chienyu Huang[*], Dipanjan Gope[+], Bibhu Nayak[+], Joe Sivaswamy[+], Harikiran Muniganti[+]

[*]Texas Instruments Incorporated, Dallas, TX, USA, [+]Simyog Technology, Pvt., Ltd.

Session T-XIV

RF and Advanced Packaging

5:50 - 6:50

Room: Conference Hall

- T-XIII.1. **Analytical Time-Domain Models for the Analysis of Tapered Differential Multibit TGVs for 3D ICs**

  Ajay Kumar, ROHIT DHIMAN   NIT Hamirpur

- T-XIII.2. **Packaged Cost-Effective Millimeterwave Air-Filled SIW Components for Array Feed Networks**

  Laura Van Messem, Arno Moerman, Olivier Caytan, Dries Vande Ginste, Hendrik Rogier, Sam Lemey   Ghent University

- T-XIII.3. **137-150 GHz Magnetically Tuned Frequency Generator for 6G Wireless Communication**

  Guoqing Dong[*], Yifan Ding[*], Yizhu Shen[+], Sanming Hu[+]   [*]Southeast university, [+]Southeast university

Session T-XV

6:50 - 8:50   **Gala Dinner**

Wednesday, December 13, 2023

Session W-I

8:30 - 9:00

Keynote-3: Advanced Packaging and Heterogeneous Integration: Past, Present & Future

Room: Conference Hall

Speaker: Madhavan Swaminathan

Session W-II

9:00 - 10:40

Telecommunications and Autonomous Systems

Room: Conference Hall

- W-II.1. **Indoor Localization of User Equipment in a 5G Ecosystem using a Hybrid Localization Approach**

  Mohammad Farhaan, Jeelany Aunowar and Vandana Bassoo — University of Mauritius

- W-II.2. **Energy Efficiency of 5G Massive MIMO Base Stations in Dense Urban Environments**

  Bhuvaneshwar Doorgakant and Tulsi Pawan Fowdur — University of Mauritius

- W-II.3. **Design and Implementation of a low-cost automatic Cardiopulmonary Resuscitation (CPR) system**

  Nihal Toolsee, Mahendra Gooroochurn — University of Mauritius

- W-II.4. **Design and Implementation of an Autonomous Mobile Robot for Fabric Fluff Collection**

  Guru-Abhivaysh Seesurun, Mahendra Gooroochurn — University of Mauritius

- W-II.5. **Driving Assistance System at T- Junctions in Mauritius using V2V Communication**

  Rajkumarsingh Bhimsen — University of Mauritius

W-III: Coffee Break

10:40 - 11:00

Room: Conference Hall

Session W-IV

Numerical Methods for Packaging

11:00 - 12:00

Room: Conference Hall

- W-IV.1. **Time Domain Partial Elements: A New Paradigm for Improved PEEC Models**

Giulio Antonini[*], Fabrizio Loreto[*], Daniele Romano[*], Jonas Ekman[+], Martin Stumpf[**], Albert Ruehli[++]

[*]University of L'Aquila, [+]University of Lulea, [**]University of Brno, [++]Missouri University of Science and Technology

- W-IV.2. **A Semi-Analytical Approach for Variability-Aware Jitter Estimation**

Challa Bhavani Sankar[*], Tripathi Jai Narayan[+], Achar Ramachandra[**]

[*]Indian Institute of Technology Jodhpur, [+]Indian Institute of Technology Jodhpur , [**]Carleton University

- W-IV.3. **Temperature-Dependent MRTD Model for Transient Analysis of Coaxial-TGVS IN 3Ds**

K Madhu kiran, Rohit Dhiman

National Institute of technology, Hamirpur

Session W-V

EDA-3: Siemens

12:00 - 12:15

Room: Conference Hall

Pre-layout early-stage workflows for signal integrity analysis and thermal analysis for Chiplet-based designs - Subramanian Lalgudi

12:15 - 1:00   W-VI: Lunch

Session W-VII

EDA-4: Ansys

1:00 - 1:30

Room: Conference Hall

Next Generation Package design with Chip Package codesign methodology - Vamsi Krishna

Session W-VIII

1:30 - 2:00 **Keynote-4: Renewable Energy for Mauritius: A Sustainable Pathway towards 2030**

Speaker: Robert Ah King

Session W-IX

Test and Measurements

2:00 - 3:20

Room: Conference Hall

- W-IX.1. **Simulation vs Measurement: Comparing PCB design simulations data with the board measured data , importance of the modeling accuracy for better corelation at multi GHz frequencies**

  Rajesh Badala Jagadeesh[*], Venkatesh Ramashastry[*], Bharath Ramprasad[+], Surya Prakash Rao Bengaluru Srihari[*], Pavan Gulur Srinivas[+]

  [*]Tessolve Semiconductor, [+]Tessolve Semiconductor

- W-IX.2. **An automatic channel test scheme for multi-chip stacked package with inductively coupled interconnection**

  Yang Cui[*], Zhuo Yang[*], Jie Xiong[+], Wenwen Cai[*], Hao Gao[+], Wei Zou[*], Li Zhang[+]

  [*]Hubei University of Technology, School of Schience, [+] Hubei University of Technology, School of Schience

- W-IX.3. **Fixture De-Embedding Challenges for Short 2xThru Structure**

  Tsiklauri Giorgi [*], Tsintsadze Giorgi[+], Dikhaminjia Nana[**], Drewniak James [+], Tsiklauri Mikheil[+], Oniani Salome[**], Zai Richard [++]

  [*]University of California Davis, [+]Missouri University of Science and Technology, [**]Alte University, [++]PacketMicro Inc

- W-IX.4. **A Low-Cost Design for Non-Standard LIN Signal Generator Based on Transistors**

  Song Ping Yang[*], Lan Chen[*], Mei Song Tong[+]

  [*]Shanghai Institute of Technology,
  [+]Tongji University

3:20 - 3:30   W-X: Coffee Break

Session W-XI

Signal Integrity

3:30 - 4:30

Room: Conference Hall

- W-XI.1. **Signal Integrity Analysis of High-speed PCIe Channel with Board-to-Board Interconnect for High-Performance Server**

  Seongguk Kim[*], Keeyoung Son[*], Jiwon Yoon[*],
  Taein Shin[*], Keunwoo Kim[*], Boogyo Sim[*],
  hyunwook Park[+], Joonsang Park[*], Seonguk Cho[*],
  Jihun Kim[*], Haeyeon Kim[*], Joungho Kim[*]

  [*]Korea Advanced Institute of Science and Technology (KAIST), [+]Missouri University of Science and Technology (MST)

- W-XI.2. **Space Mapped Neuromodeling for Fast & Accurate Signal Integrity Analysis of Rough On-chip Copper Interconnects**

  Suyash Kushwaha, Surila Guglani, Nastaran Soleimani, Sunil Pathania, Somesh Kumar, Riccardo Trinchero, Sourajeet Roy, Rohit Sharma

  [*]Indian Institute of Technology Ropar, [+] Indian Institute of Technology Roorkee, [**]Politecnico di Torino, [++]Indian Institute of Technology Ropar , [***]Indian Institute of Information Technology Gwalior, [+++]Indian Institute of Technology Roorkee

- W-XI.3. **Minimum Cursors Selection in Statistical Method for Eye Diagram Simulation in a High-Speed Link Nonlinear System**

  Bobi Shi, Jose Schutt-Aine   UIUC

Session W-XII

Power Integrity

4:30 - 5:50

Room: Conference Hall

- W-XII.1. **A Two-Level Waveform Relaxation Approach for System-Level Power Delivery Verification**

Alessandro Moglia[*], Antonio Carlucci[*], Stefano Grivet-Talocia[*], Scott Mongrain[+], Sid Kulasekaran[+], Kaladhar Radhakrishnan[+]

[*]Politecnico di Torino, [+]Intel Corporation

- W-XII.2. **Power Integrity Design of Mobile 3D-IC Based on the Allocation of Optimal Number of TSV, BGA, and Via**

Hyunwoong Kim[*], Seonghi Lee[+], Dongryul Park[*], Jungil Son[**], Yongho Lee[**], Sungwook Moon[**], Jiseong Kim[*], Seungyoung Ahn[+]

[*]Korea Advanced Institute of Science and Technology, [+] Korea Advanced Institute of Science and Technology, [**]SAMSUNG Foundry

- W-XII.3. **Time Delay Compensation to improve the Transient response of Fully Integrated Voltage Regulators in Microprocessors**

Amit Kumar[*], Srinivasan Govindan[+], Srikrishnan Venkataraman[+], Schaef Christopher[+], Seshasayee Nikhil[+]

[*]Intel Technology India Pvt. Ltd, Bangalore, India, [+]Intel Technology India Pvt. Ltd, Bangalore, India

- W-XII.4. **3D-IC Power Distribution Network (PDN) Impedance Prediction using Deep Learning (DL)**

Park Dongryul[*], Ryu Seunghun [*], Kim Hyunwoong[*], Lee Seonghi[*], Song Sangsub[+], Yong Seokbeom[+], Ahn Seungyoung[*]

[*]Korea Advanced Institute of Science and Technology, [+]SAMSUNG Electronics

Session W-XIII

Awards and Conference Wrap-up

5:50 - 6:00

Room: Conference Hall

Thursday, December 14, 2023

Session R-I

9:00 - 10:00

EDAPS Committee Meeting

Room: Conference Hall

10:00-11:00   **University of Mauritius visit**

11:00-13:00   **Island tour and lunch**