# 2024 IEEE EDAPS Technical Program

## Taj Yeshwantpur, Bangalore

## 17th – 19th December 2024

## Day 1: Tutorials

(Chairs: Jai Narayan Tripathi and Sourajeet Roy)

**9:00 AM - 10:00 AM:**
Tutorial 1: Machine Learning-based methodologies for the design of modern RF and microwave systems
Domenico Spina, Vrije Universiteit Brussel
Tom Dhaene, Ghent University

**10:00 AM - 11:00 AM**
Tutorial 2: Recent advances in 5G circuits and systems
Venkata Vanukuru, Global Foundries, India

**11:00 - 11:30 AM**
Coffee Break

**11:30 - 12:30 PM**
Tutorial 3: System-Level Predictive EMI/EMC Modeling
Rajen Murugan, Texas Instruments, Inc. and Dipanjan Gope, IISc, Bangalore

**12:30 - 2:00 PM**
Lunch

**2:00 - 3:00 PM**
Tutorial 4: MOSFET Modeling: An Industry Perspective
Shruti Mehrotra, Global Foundries

**3:00 - 4:00 PM**
Tutorial 5: Design Co-packaged Optics with Ansys Multiphysics Solutions
Nikhil Dhingra and Anushruti Jaiswal, Ansys Inc.

**4:00 - 4:30 PM**
Coffee break

**4:30 - 5:30 PM**
Tutorial 6: Why are Semiconductor Packaging & Heterogeneous Integration taking Center Stage for continuing Moore's Law?
Madhavan Swaminathan, Penn State University

**6:30 - 8:30 PM**
Reception

## Day 2: Keynotes, Technical Sessions, Poster Session

**9:00 AM - 9:10 AM**
**Opening ceremony** (Chair: Rohit Sharma)

**9:10 AM - 10:10 AM**
**Keynote 1: Unleashing the Power of Advanced Packaging by Connecting System Design Optimization and Smart Manufacturing**
Pradeep Vempaty, Micron
(Chair: Rohit Sharma)

**10:10 AM - 11:30 AM**
**Session 1: Heterogeneous Integration I**
(Chair: Ruey-Beei Wu and Ram Achar)

**10:10 AM - 10:30 AM**
Paper 1: Signal Integrity Analysis with Compliance Test of USB4.0 Gen3 with Reference Channels & IBIS-AMI Models
Amit Jangale, Varun Agarwal
Keysight Technologies

**10:30 AM - 10:50 AM**
Paper 2: Signal-Integrity Assurance in HBM Links with Temperature-Dependent Interconnections
Ju-Ching Chien, Chien-Min Lin, Ruey-Beei Wu
National Taiwan University

**10:50 AM - 11:10 AM**
Paper 3: Design and Analysis of Twin Tower High Bandwidth Memory (HBM) Architecture for Large Memory Capacity and High Bandwidth System
Kim Taesoo, Yoon Jiwon, Choi Seonguk, Kim Haeyeon, Suh Haeseok, An Hyunjun, Ahn Jungmin, Park Hyunah, Kim Joungho
Korea Advanced Institute of Science and Technology

**11:10 AM - 11:30 AM**
Paper 4: UCIeA Signal Integrity System Level Analysis for 3DIC AI Chip
Shantanu Swami, Manjunath Jayasimha
Intel Inc.

**11:30 - 11:50 AM**
**Coffee Break**

**11:50 AM - 11:30 AM**
**Session 2: Modeling for EMC**
(Chairs: Tom Dhaene and Sourajeet Roy)

**11:50 AM - 12:10 PM**
Paper 1: Computationally Efficient System-Level Modeling for Open-Loop Bulk Current Injection (BCI) Testing
Jie Chen
Texas Instruments

**12:10 PM - 12:30 PM**
Paper 2: Surface Modeling using RWG Basis Function for Radiated Emission Prediction
Samipendu Das, Dipanjan Gope, Harikiran Muniganti
Indian Institute of Science

**12:30 PM - 12:50 PM**
Paper 3: A Fast Algorithm for the Near-Field Radiation Assessment of Interconnects
Martijn Huynen, Kamil Yavuz Kapusuz, Victor Verstraete, Alessandro Felaco, Dries Vande Ginste
Ghent University/IMEC

**12:50 PM - 1:10 PM**
Paper 4: Radiated Emission Behavioral Modeling and Mitigation for Ungrounded Heatsink by VRs Inductor
Rajiv Panigrahi, Rajendra Vrukshavai, S P, Shyju, Shashidhara Shivakumara
Intel Inc.

**1:10 PM - 2:30 PM**
**Lunch (+ TPC Meeting)**

**2:30 PM - 3:30 PM**
**Panel Session on Indian Semiconductor Mission**
**Panellist: Arun Chandrasekhar (Intel Inc.), Ravi Bhatkal (Macdermid Alpha), Raghu Panicker (Kaynes Tech.) and Nilesh Badwe (IIT Kanpur)**
(Moderator: Rohit Sharma)

**3:30 PM - 3:50 PM**
**Coffee Break**

**3:50 PM - 5:10 PM**
**Session 3: Signal and Power Integrity I**
(Chairs: Riccardo Trinchero and Ruey-Beei Wu)

**3:50 PM - 4:10 PM**
Paper 1: A Hybrid GRU-KBNN based Approach for Estimating Jitter in a Chain of CMOS Inverters
Ahsan Javaid, Ramachandra Achar, Jai Tripathi
Carleton University and IIT Jodhpur

**4:10 PM - 4:30 PM**
Paper 2: Semi-Analytical Analysis on Impact of Ground Bounce on Logic-High at the Output Response of the Inverter Circuit
Anuj Kumar, Jai Narayan Tripathi
IIT Jodhpur

**4:30 PM - 4:50 PM**
Paper 3: Power supply noise-induced performance degradation in transmitter: An analysis of eye height and vertical eye closure at 106.25 Gbps data rate
Kalyan Vaddagiri, Sameer Joshi
Cisco Systems India Pvt. Ltd

**4:50 PM - 5:10 PM**
Paper 4: Investigating PSN and GBN Induced Jitter at Different Stages of a Chain of CMOS Inverters
Vinod Kumar Verma (student), Dinesh Junjariya, Jai Narayan Tripathi
IIT Jodhpur

**6:00 PM - 7:00 PM**
**Poster Session**
(Chairs: Ram Achar and Domenico Spina)

**Poster 1:** Signal Integrity (SI) Analysis and Optimization of a 20-slot Aggregation Router and Recurring Fabric Link Field Failures
Balaji G, Bala Sirish Chaturvedula, Sameer Joshi
Cisco Systems India Pvt. Ltd

**Poster 2:** Parasitic Effects Prediction in On-Chip-Antennas
Shilpa Pavithran, Elizabeth George, Alex James
Digital University Kerala

**Poster 3:** Challenges Solutions with System Analysis for UCIeA Power Delivery and Power Integrity in 3DIC AI Chip
Manjunath Jayasimha, Rishik Kola, Himanshu Kandpal
Intel Inc.

**Poster 4:** Modeling and Analysis of Crosstalk Noise for Analog Interconnects in Server Microprocessors
Amit Kumar, Amit Bhaiji, Srinivasan Govindan, Srikrishnan Venkataraman, Shobha, Strnad Bryan, Thomas Bozic, Tal Goihman, Trevor A Miller
Intel Inc.

**Poster 5:** Estimation of Power Supply Induced Jitter in Push-Pull Drivers in MIPI C-PHY
Vinod Kumar Netad, Jai Narayan Tripathi, Tzong-Lin Wu
National Taiwan University and IIT Jodhpur

**Poster 6:** Parametric Study of Factors Affecting PMIC-QFN under Temperature Cycling for DIMM System
Christopher Glancey, Yeow Chon Ong, Hong Wan Ng
Micron Technology

**Poster 7:** Linear Regression Machine Learning Model Development for Package Warpage
Fa Xing Che, Yeow Chon Ong, Prasad Nagavenkata Nune, Hong Wan Ng, Sunil Kumar Panigrahy
Micron Technology

**Poster 8:** Client DDR5 UDIMM timing margin analysis, debug and improvements at 5600Mbps
Anil Bindu Lingambudi, Sireesha Yettella, Zhenglong (Aaron) Wu, Justin Hsieh
Intel Corporation

**Poster 9:** Root cause analysis to predict the die cracks in the multichip package
Anil Raj Purra, Harsh Kumar, Venkata Rama Satya Pradeep Vempaty, Ken Tamala
Micron Technology

**Poster 10:** Robust Design Optimization applied to unit warpage analysis of exposed die flip-chip package
Chih-Yen Su, Nai-Jen Hsuan, Ying-Hsi Lin
Realtek Semiconductor Corp.

**Poster 11:** Application of Pradovera's Algorithm for Adaptive Frequency Sampling in Electromagnetic Simulation
T N Shilpa, Rakesh Sinha
National Institute of Technology Rourkela

**Postern 12:** Performance of Plasma Treated 2D MoS2 Synaptic Memristor for Neuromorphic Computing
Kanupriya Varshney (student), Rohit Sharma, Devarshi Mrinal Das, Brajesh Rawat
IIT Ropar

**7:30 PM – 9:00 PM**
Gala Dinner

## Day 3: Keynotes, Technical Sessions, Awards

**9:00 AM – 9:45 AM**

**Keynote 2: Assessing the Risk of Chip-Package Interaction Failures in Advanced Packaging: Modeling Crack Initiation and Growth in BEOL Structures**

Ganesh Subbarayan, Purdue University

(Chair: Rohit Sharma)

**9:45 AM – 10:30 AM**

**Keynote 3: On Scaling from Circuits to Systems**

Jairam Sukumar, Qualcomm Inc.

(Chair: Rohit Sharma)

**10:30 AM – 10:50 AM**

**Coffee break**

**10:50 AM – 11:50 AM**

**Session 4: Heterogeneous Integration II**

(Chairs: Hideki Sasaki and Jai Narayan Tripathi)

**10:50 AM – 11:10 AM**

Paper 1**:** Transient Analysis of Through Package Coaxial Vias in Glass Interposers Based on SBTD Method

K Madhu Kiran (student), Suyash Sachdeva (student), Rohit Dhiman

National Institute of Technology Hamirpur

**11:10 AM – 11:30 AM**

Paper 2: Signal Integrity Analysis of Ultra-scaled Copper-Graphene Heterogeneous Interconnect Structures

Suyash Kushwaha (student), Devarshi Mrinal Das, Sourajeet Roy, Rohit Sharma

IIT Ropar

**11:30 AM – 11:50 AM**

Paper 3: Spacer Optimization using a Neuro-PSO Approach for Improving FinFET Repeater Performance in On-Chip Global MLGNR Interconnects

Asha Kumari Jakhar (student), Avirup Dasgupta, Rohit Sharma, Sourajeet Roy

IIT Roorkee and IIT Ropar

**11:50 AM – 1:10 PM**
**Session 5: Signal and Power Integrity II**
(Chairs: Ram Achar and Nikita Ambasana)

**11:50 AM – 12:10 PM**
Paper 1: Multi-objective Optimization of FIVR Control Loop
Srinivasan Govindan, Srikrishnan Venkataraman, Beomseok Choi, Amit Kumar
Intel Technology India Pvt Ltd

**12:10 PM – 12:30 PM**
Paper 2: A quicker PSO convergence for decaps placement in a power delivery network
Kamlesh Gupta, Mridul Gupta (student), Jai Narayan Tripathi
IIT Jodhpur

**12:30 PM – 12:50 PM**
Paper 3: Modeling of Eye Diagram for Jitter Estimation in the Presence of Ground Bounce
Anuj Kumar (student), Jai Narayan Tripathi
IIT Jodhpur

**12:50 PM – 1:10 PM**
Paper 4: Capacitive noise coupling modelling from power plane to signal trace at VRM region and its mitigation
Rajiv Panigrahi, Raghav Kurni, A V Meiyappan, Nilesh Kumar Tiwari, Muthukumaran Durairaj
Intel Inc.

**2:30 PM – 4:10 PM**
**Session 6: Machine Learning and Macromodeling**
(Chairs: Tom Dhaene and Riccardo Trinchero)

**2:30 PM – 2:50 PM**
Paper 1: GPU-based PRIMA Algorithm for Passive Model Order Reduction
Rayeed Anando (student), Anuran Bhunia (student), Ram Achar
Carleton University

**2:50 PM – 3:10 PM**
Paper 2: Machine Learning Assisted Evolutionary Algorithm for Device-Circuit Multi-Objective Co-optimization of Actively Shielded MWCNT Interconnects
Km Dimple (student), Avirup Dasgupta, Sourajeet Roy, M. Ehteshamuddin
IIT Roorkee

**3:10 PM – 3:30 PM**
Paper 3: Machine Learning based Netlisting for Hand-drawn Circuit Schematics with Subcircuits for High-Speed Applications
Anuj Mathur (student), Ram Achar
Carleton University

**3:30 PM – 3:50 PM**
Paper 4: Compressed SPICE-compliant IC Models via Machine Learning Kernel Regression
Marco Atlante, Riccardo Trinchero, Tommaso Bradde, Paolo Manfredi, Igor Stievano
Politecnico di Torino

**3:50 PM – 4:10 PM**

Paper 5: Machine Learning Based Inverse Model for Identifying Transmission Line Network Parameters from Tabulated Frequency-Domain Data
Mohd Yusuf (student), Avirup Dasgupta, Sourajeet Roy
IIT Roorkee

**4:10 PM – 4:30 PM**

**Session 7: Awards and closing**
(Chairs: Rohit Sharma, Ram Achar and Tom Dhaene)