17th IEEE Electrical Design of Advanced Packaging and Systems (EDAPS) Symposium

17th December – 19th December, 2024

Bengaluru, INDIA

Call for Papers

The IEEE Electrical Design of Advanced Packaging and Systems (EDAPS) Symposium is the premier international conference held in the Asia-Pacific region to share the recent advances in the design, modeling, simulation, and measurement related to the electrical issues arising at the chip, package, and system levels. Covering the paper presentations, industry exhibitions, workshops, and tutorials, EDAPS 2024 will be held at the **Taj Yeshwantpur, in Bengaluru, India from December 17 to 19, 2024**. The technical program of the symposium will not only focus on the current issues but also brings out the topics on IC design, SiP/SoP packaging, EMI/EMC and most importantly the challenging issues in advanced 3D-IC, chiplet and heterogeneous integration, and the application of machine learning in EDA. For further information, please consult the web site at http://edaps.org.

IMPORTANT DATES

Paper Submission Portal Open: **July 15, 2024**

Paper Submission Portal Closed: **August 31, 2024**

Acceptance Notification: **September 30, 2024**

http://edaps.org

IEEE

IEEE ELECTRONICS PACKAGING SOCIETY

TOPICS

- 3D-ICs/TSVs/Interposers
- Testing on 3D-IC and SiP
- Signal and Thermal Integrity
- Power Integrity and Power Distribution Networks (PDNs)
- Computational Electromagnetics and Multi-physics Modeling
- Thermal Management Design for 3D-ICs and SiP
- Design and Modeling for High-speed Channels and Interconnects
- High-Speed Serial Links Jitter Budgeting
- Jitter Analysis and Modeling Algorithms and Tools
- Time / Frequency Domain Measurement Techniques
- Power Supply Induced Jitter and Transfer Functions
- Nanoelectronics for 3D-ICs and SiP
- Machine Learning Applied to Packaging
- Active Devices and Circuit Modeling Technologies
- Electronic Packages, SiP/ SoP
- IC and Package Level EMC
- Antennas in Packages (AiP)
- RF/mm-wave and THz Packages
- Miniaturized and Embedded Passives
- Power Electronic Packages
- Advanced Simulation Tools and CAD
- Substrate Technology for Packages and PCBs
- Electrical Design of Flexible Devices and Sensing
- 2-D Materials for 3D-ICs and SiP
- 3-D ICs and SiP Reliability
- Electrical Design for 5G Wireless Communication
- SI/PI Analysis of High-Speed Channels
- Others

STUDENT TRAVEL GRANTS - A limited number of travel grants will be provided to support students of accepted papers. Selection will be based on papers submitted and requires paper presentation by the student at the conference.

PAPER SUBMISSION

All papers should be submitted electronically in **two-column and three-page** PDF file format. All submissions must be made through EDAPS website (http://edaps.org). A Microsoft Word template is available on the symposium website. Hardcopy submission will NOT be accepted. Submitted manuscripts should be camera ready and compliant with the general standards of the IEEE, including appropriate referencing. Non-compliant manuscripts will not be considered for review. An IEEE copyright transfer form completed with paper title, author(s) name(s) and authors' signatures should be submitted at the time of the paper submission. Files with scanned signatures are considered valid documents. Please check back with the symposium website (http://edaps.org) for updates on the paper submission. **Selected papers will be invited for publication in the IEEE Transactions on Components, Packaging and Manufacturing Technology.**